Cineca
TRAINING
High Performance
Computing 2017

IntraNode Optimization

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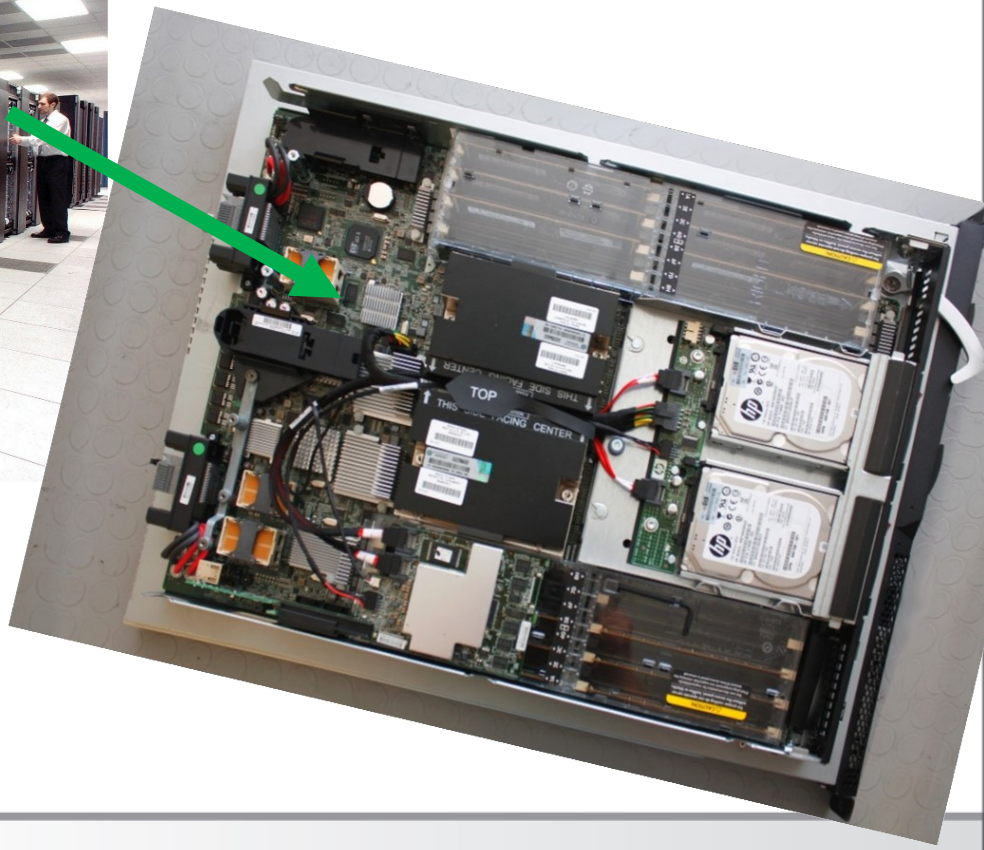
CINECA

Intranode Optimization



Are you ready?

Today you become

Software Mechanic!!

Explore the engine!

Intel Vtune Profiler

PROFILING SHOWS THE

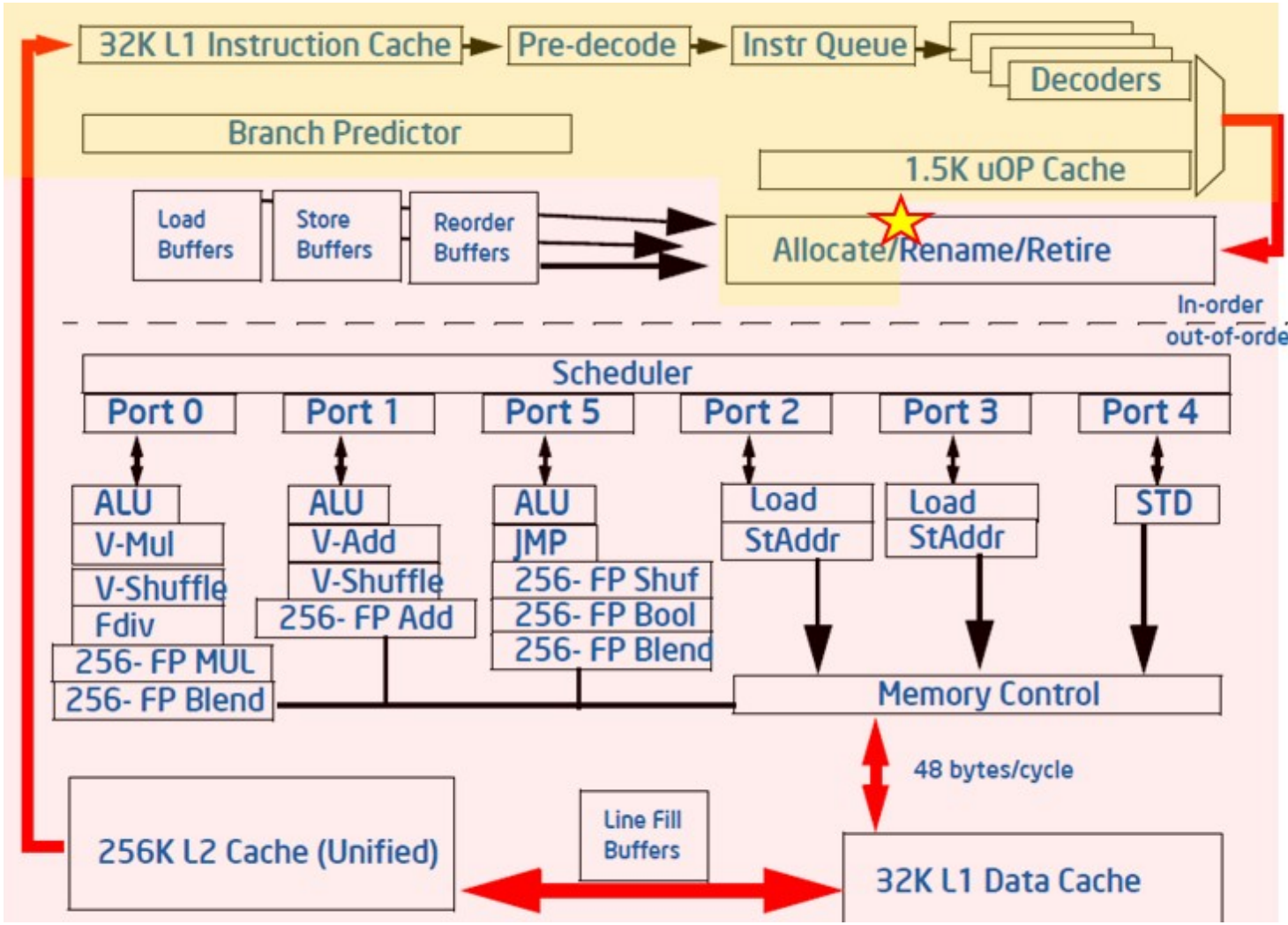
PERFORMANCE OF

HARDWARE AND SOFTWARE COUPLED

Modern Processor Pipeline

Front END

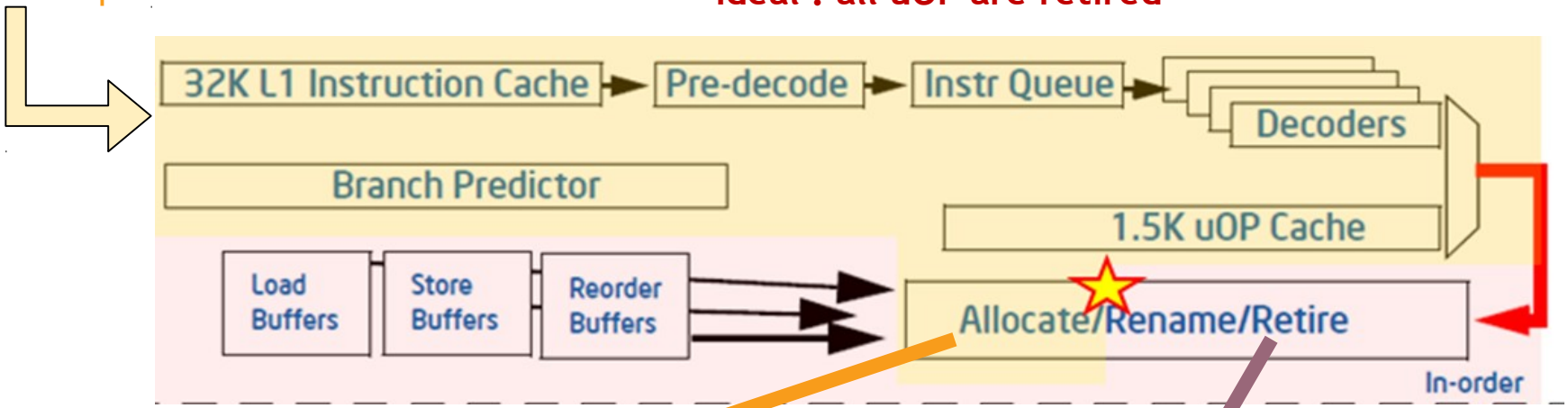
Back END



Front End

Compiled CODE

Ideal : all uOP are retired



Allocation:

process that

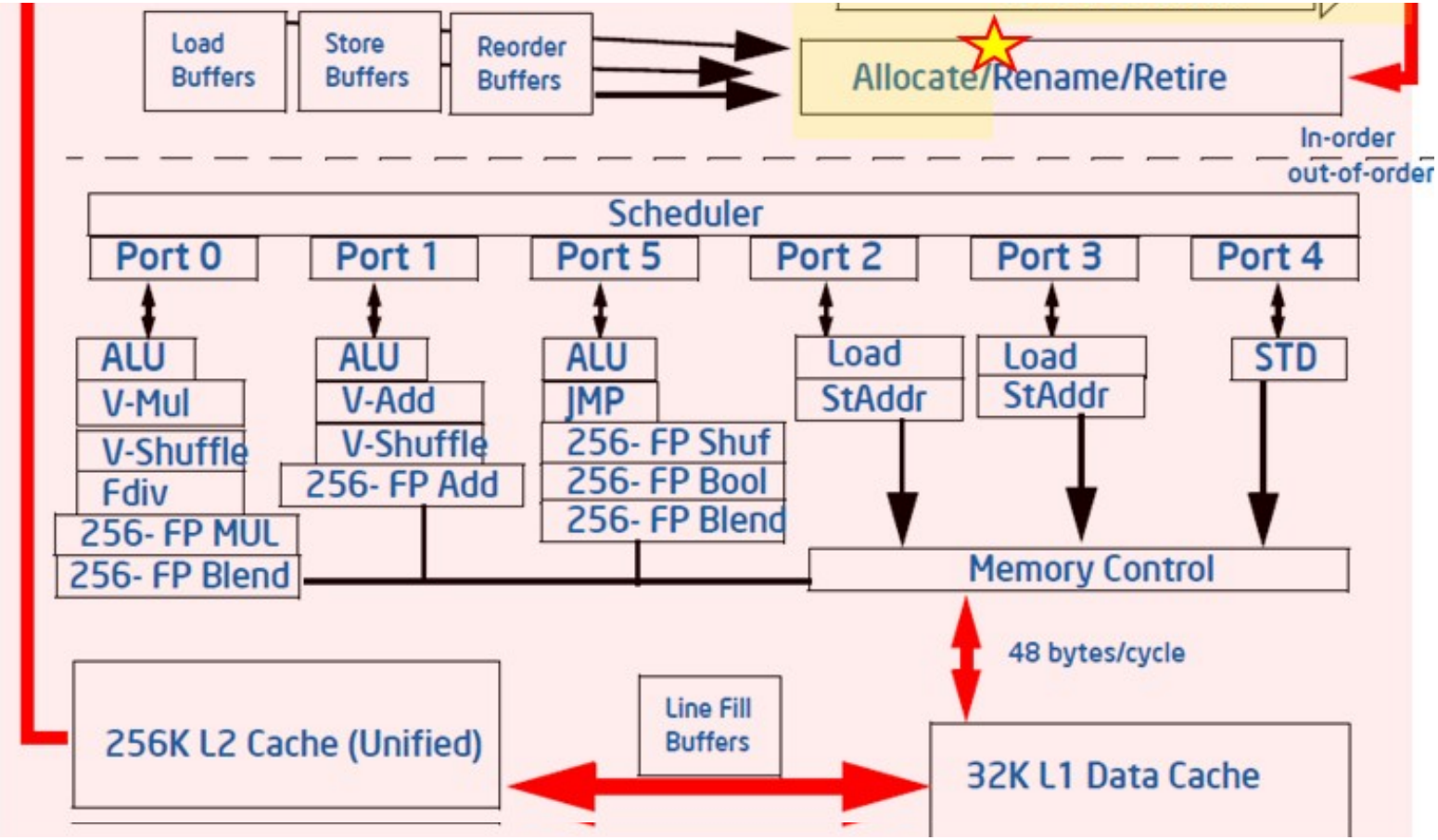
fed the BE of uOP

Retirement:

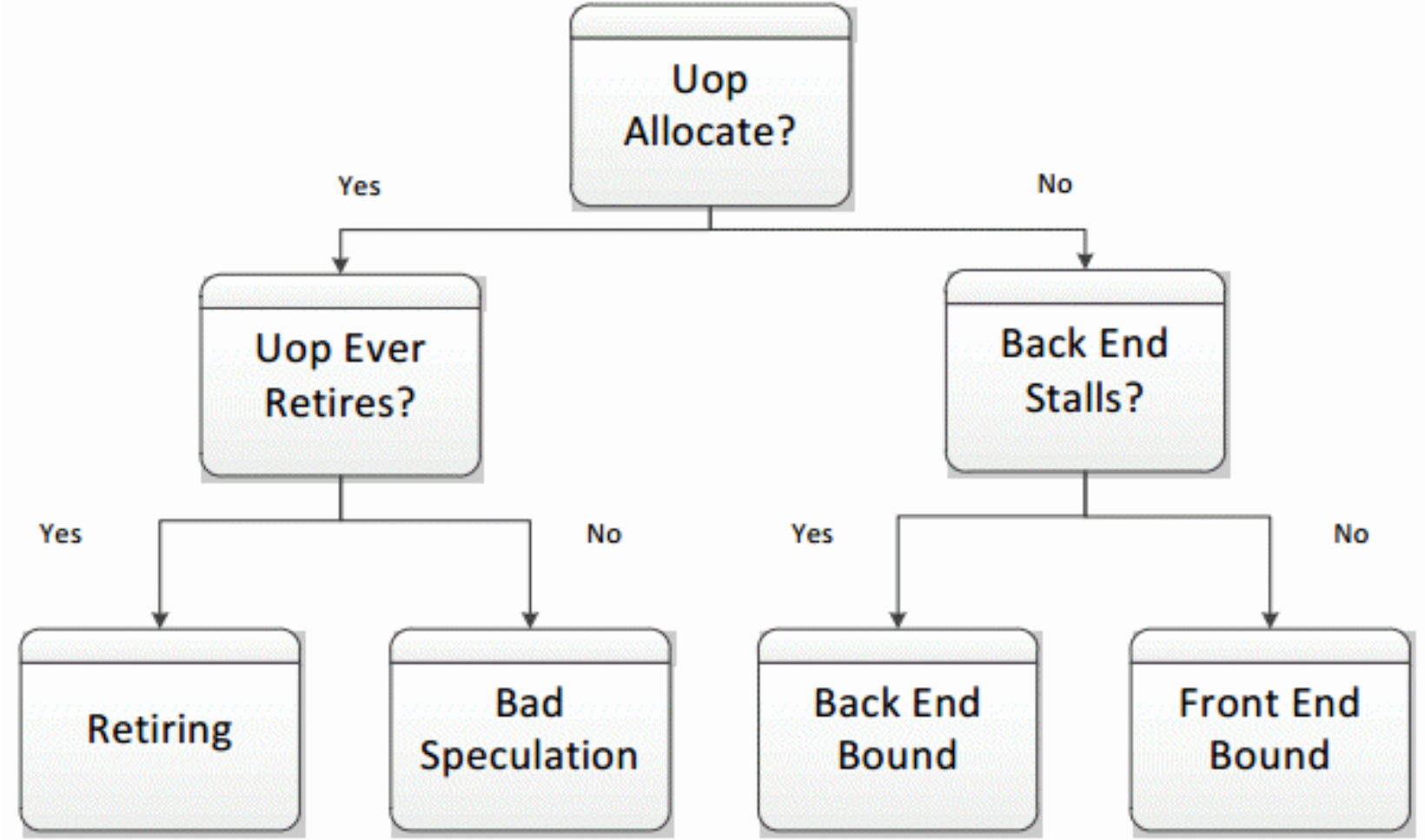
The completion of a uOp's execution. The results are committed to the architectural state.

4 uOP/cycle(pipeline slot) => *CPI* = 0.25

Back End


Load Buffers
Store Buffers
Reorder Buffers
Allocate/Rename/Retire
In-order
out-of-order
Scheduler
Port 0
Port 1
Port 5
Port 2
Port 3
Port 4
ALU
V-Mul
V-Shuffle
Fdiv
256- FP MUL
256- FP Blend
ALU
V-Add
V-Shuffle
256- FP Add
ALU
JMP
256- FP Shuf
256- FP Bool
256- FP Blend
Load
StAddr
Load
StAddr
STD
Memory Control
48 bytes/cycle
256K L2 Cache (Unified)
Line Fill Buffers
32K L1 Data Cache

Intel's Diagram



FE,Retiring and Bad Speculation

Retiring : the performance issues are probably due to an heavy use of micro sequencer (assistant generator of long stream of uOPs)

Bad Speculation : when the pipeline is busy fetching and executing non-useful operations due to incorrect speculation.

Front End: problem related to code layout, try to solve using PGO(Profiling guided optimization).

PROFILE GUIDED OPTIMIZATION

icc **-prof_gen** code.c

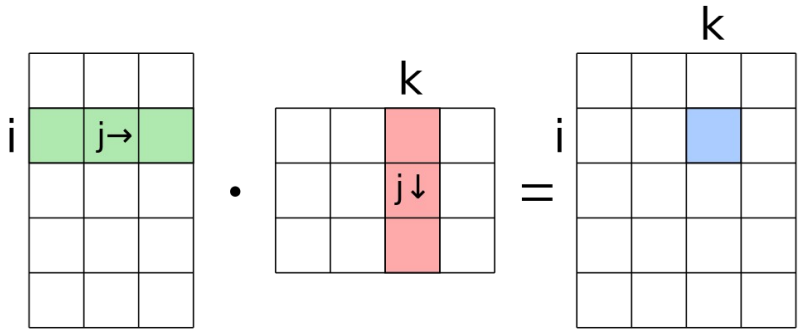
icc **-prof_use** code.c

Launch code.xx

On typical dataset

What is the difference?

Matrix Mul

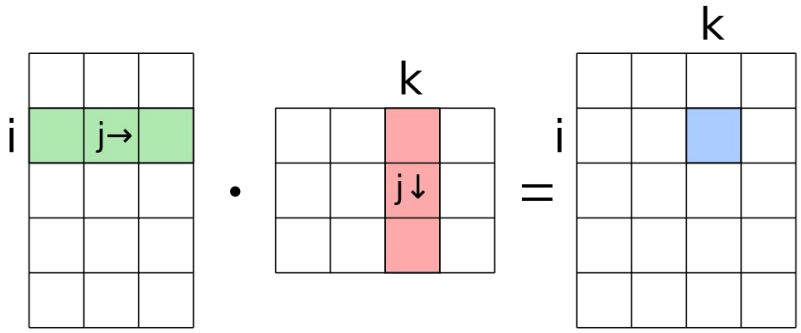


AXPI

a*X+Y

What is the difference?

Matrix Mul



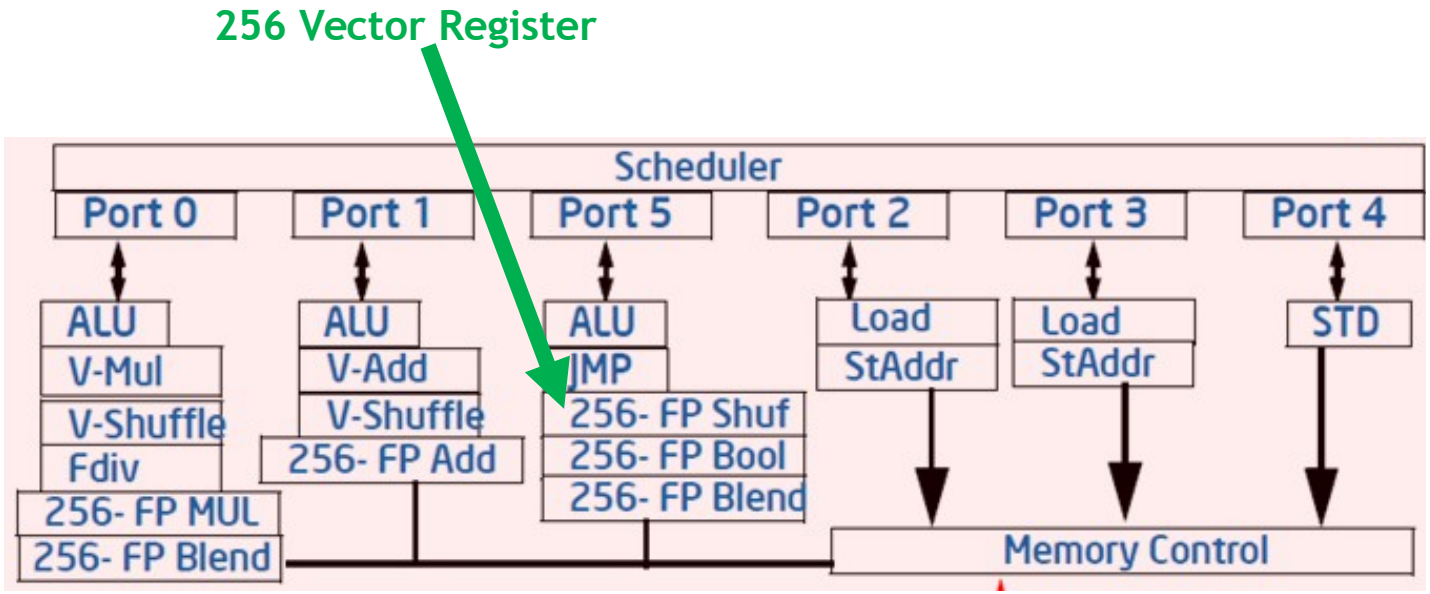
CORE BOUND

AXPI

a*X+Y

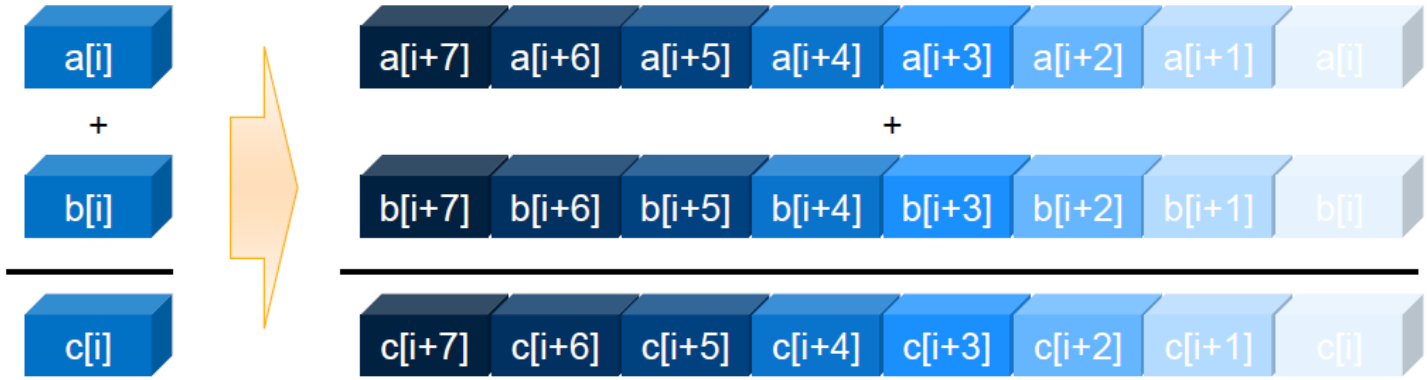
MEM BOUND

Increase Performance

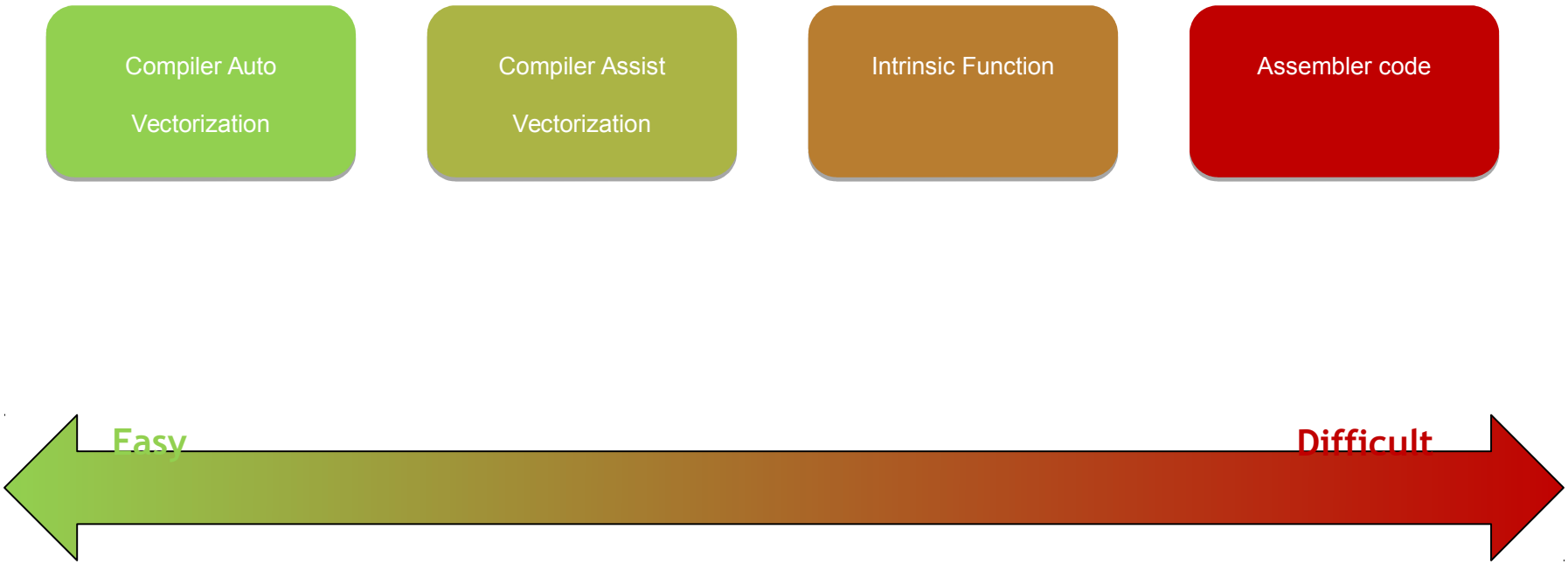


Single Instruction Multiple Data

```
for(i = 0; i <= MAX;i++)
    c[i] = a[i] + b[i];
```



Many Ways


Compiler Auto
Vectorization
Compiler Assist
Vectorization
Intrinsic Function
Assembler code
Easy
Difficult

Compiler AutoVectorization

icc -x<ARCH>

icc -no-vec

icc -ax<ARCH1>,<ARCH2>

CINECA MARCONI ARCH = avx2

To see code optimization report

icc -qopt-report 5

Reason for Vectorization Fails

Data dependencies

Wrong Alignement

Non-unit stride access

Non Vec Math functions

Function calls

Loop body

Too complex

Data Alignment

Data alignment means putting the data at

a memory address equal to some multiple of

the word size (AVX 256 bit).

```
void * _mm_malloc(int size, int word)
```

Remember to compiler that an array is aligned `__assume_aligned(var,word);`

Data Dependency

Flow dependence

```
for(int i;..){
        X[i] =
         … = X[i]
}
```

Anti dependence

```
for(int i;..){
         … = X[i]
          X[i] = …
}
```

Output dependence

```
for(int i;..){
          X[i] = …
          X[i] = …
}
```

DOWNLOAD RCM : https://hpc-forge.cineca.it/svn/RemoteGraph/branch/multivnc/build/dist/Releases/?p=817

Exercise 1 : VTune Profiling

```
module load autoload vtune
```

```
qsub -I -l select=1:ncpus=1:mem=20GB -l walltime=00:30:00 -q R457635 -A train_scA2017 -X
```

Exercise 2 : Vectorization

```
module load autoload vtune python/3.5.2
```

```
source /marconi_scratch/userinternal/epascol1/adv_py_school/bin/activate
```